board is subjected to the thermal shock test or reflow.

(Seventh Embodiment)

A method and apparatus for mounting an electronic component of, for example, an IC chip on a circuit board and an electronic component unit or module of, for example, a semiconductor device in which the IC chip is mounted on the board by the mounting method, according to a seventh embodiment of the present invention will be described next with reference to Fig. 12 and Fig. 13. According to this seventh embodiment, the stress of the IC chip 1 and the circuit board 4 in the first embodiment can be alleviated when the thermosetting resin is hardened after the bonding of the IC chip 1 to the circuit board 4.

In the seventh embodiment, the bump 3 formed on the electrode 2 of the IC chip 1 by the wire bonding is aligned in position with the electrode 5 of the circuit board 4 without leveling the bump with interposition of a solid or semi-solid anisotropic conductive film sheet 10 or a thermosetting adhesive 6b obtained by mixing an insulating resin 6m with an inorganic filler 6f. The IC chip 1 is pressed against the circuit board 4 with a pressure force P1 of not smaller than 80 gf per bump in the case of a ceramic board while heating the IC chip 1 from its rear surface side by the tool 8 heated to a specified temperature of, for example, about 230°C to correct the

warp of the board 4, and the anisotropic conductive film sheet 10 or the thermosetting adhesive 6b interposed between the IC chip 1 and the circuit board 4 is hardened by the heat. Next, assuming that the total time is, for example, 20 seconds, then, after a lapse of a specified time t1, i.e., after a lapse of five to 10 seconds being one-fourth or one-half the time, also depending on the reaction rate of the material, or in other words, before the reaction rate of the material reaches 90%, the pressure force is reduced to a pressure P2 lower than the pressure P1 to alleviate the stress when the thermosetting adhesive 6b is hardened, and the IC chip 1 and the circuit board 4 are bonded together to electrically connect both the electrodes 2 and 5. Preferably, by setting the pressure P1 to 20 gf or more per bump for the reason that a minimum of about 20 gf is required for the deformation of the bump, i.e., in order to obtain the pressure required for the deformation and adaptation of the bump and force out the excessive resin from between the IC chip 1 and the board 4 and setting the pressure P2 less than 20 gf per bump in order to remove the hardening distortion unevenly distributed inside the resin before the deformation or the like of the bump, the reliability is improved. The detailed reasons are as follows. That is, the stress distribution of the thermosetting resin in the anisotropic

conductive film sheet 10 or the thermosetting adhesive 6b is increased on the IC chip 1 side and the board 4 side at the time of pressure bonding as shown in Fig. 12C.

In this state kept intact, if fatigue is repetitively given through a reliability test and normal long-term use, then the thermosetting resin in the anisotropic conductive film sheet 10 or the thermosetting adhesive 6b sometimes unable to endure the stress and may separate on the IC chip 1 side or the board 4 side. If the above state occurs, then the adhesive strength of the IC chip 1 and the circuit board 4 becomes insufficient and the bonded portion becomes open. Accordingly, by adopting a two-step pressure profile of the higher pressure P1 and the lower pressure P2 as shown in Fig. 13, the pressure can be reduced to the pressure P2 lower than the pressure P1 when the thermosetting adhesive 6b is hardened, and the stress of the IC chip 1 and the circuit board 4 can be alleviated (in other words, the degree of stress concentration can be reduced) as shown in Fig. 12D by removing the hardening distortion unevenly distributed inside the resin with the pressure P2. Subsequently, by increasing the pressure to the pressure P1, a pressure required for the deformation and adaptation of the bump can be obtained, and the excessive resin can be forced out of the space between the IC chip 1 and the board 4, improving the reliability.